CLAIMS

What is claimed is:

1. A random access memory comprising:

a memory array having a plurality of subarrays formed by chalcogenide storage elements;

a plurality of write circuits, wherein each of said plurality of write circuits includes an independent write 0 circuit and an independent write 1 circuit, wherein each of said plurality of write circuits is associated with a respective one of said plurality of subarrays;

a plurality of read circuits, wherein each of said plurality of read circuits includes a sense amplifier circuit, wherein each of said plurality of read circuits is associated with a respective one of said plurality of subarrays;

a voltage level control module, coupled to said plurality of read and write circuits, for ensuring that voltages across said chalcogenide storage elements do not exceed a predetermined value during a read or write operation such that data values stored within said chalcogenide storage elements cannot be changed erroneously and that the life of said chalcogenide storage elements can be extended.

2. The random access memory of Claim 1, wherein said write 0 circuit includes an inverter and a write 0 transistor.

3. The random access memory of Claim 2, wherein said write 1 circuit includes an inverter and a write 1 transistor.

4. The random access memory of Claim 3, wherein write 0 transistor is larger than said write 1 transistor.

5. The random access memory of Claim 1, wherein said voltage level control module further includes a post-write discharge circuit for lowering the voltage on a column that has been previously written in order to prevent any reprogramming of a chalcogenide storage element within said previously written column on subsequent read operations.

6. The random access memory of Claim 5, wherein said post-write discharge circuit includes a diode for discharging excess current to ground.

7. The random access memory of Claim 5, wherein said voltage level control module further includes a read voltage clamp circuit for establishing an acceptable voltage limit across a chalcogenide memory element to prevent parasitic effects of stored charges on a column from influencing the information stored in said chalcogenide memory element.

8. The random access memory of Claim 7, wherein said voltage level control module further includes a reference voltage circuit to provide a reference voltage for said read voltage clamp circuit and said post-write discharge circuit.

9. The random access memory of Claim 1, wherein said chalcogenide storage elements are made of chemical elements selected from a group of tellurium, selenium, antimony and germanium.

10. The random access memory of Claim 1, wherein said random access memory further includes a column decoder and a row decoder.